ABSTRACT

This invention relates to an information processing apparatus as well as to an information processing method and a program for use therewith, the apparatus being arranged to prevent a drop in its processing performance while minimizing power dissipation when a frequency-variable synchronizing clock signal CLK of the apparatus is lowered in frequency. Illustratively, if a selector block 31-2 receives a selection command "select B" which is set depending on the frequency of the synchronizing clock signal CLK and which specifies the bypassing of a holding block 12-2, then data input to and held by a holding block 12-1 on a first clock pulse of the clock signal CLK is arranged, on a second clock pulse, to pass through a selector block 31-1 and a signal processing block 13-1, bypass the holding block 12-2, pass through the selector block 31-2 and a signal processing block 13-2, and be input to and held by a holding block 12-3. This invention applies to data processing apparatuses such as CPUs, DSPs and filters as well as to buses.